instruction pointer register over an instruction pointer bus. See column 16, lines 35-37. The terms used in the teachings such as "register" and "bus" imply a multiple bit word although Figure 9 shows a single line as is common for simplified illustrations of bus lines. The purpose of the instruction pointer logic circuit as taught in the Vidwans patent is to determine instruction pointer limit violations and not to process conditional branching as claimed. See column 12, lines 60-65. Claim 1 recites in part "a plurality of first flag selectors, each first flag selector presenting a flag from a plurality of available flags". The Vidwans patent does not suggest or motivate one of ordinary skill in the art to adapt the teachings of the Kamiyama patent to process multiple available flags to arrive at a branch flag that indicates whether to branch according to the conditional instruction as claimed. The combination of the two references cited, therefore, does not include sufficient teachings to arrive at the claimed invention and withdrawal of the rejection is respectfully requested.

Claims 2-11 are rejected as rendered obvious by the combination of the Kamiyama and Vidwans patents and further in view of various others including US Pat. No. 5,408,620 to Asakawa ("the Asakawa patent"), US Pat. No. 5,479,649 to Runaldue ("the Runaldue patent"), US Pat. No. 4,742,466 to Ochiai ("the Ochiai patent"), and US Pat. No. 6,067,617 to Webb

("the Webb patent"). Claims 2-11 depend from claim 1, which for reasons presented above is believed to be patentable. Accordingly, claims 2-11 are also believed to be patentable.

With specific reference to claims 2 and 6, the Office Action suggests that the Asakawa patent teaches that multiple input logical AND operators are known. The Asakawa patent, however, does not supply the teachings absent from the combination of the Kamiyama and Vidwans patent to render claim 1 obvious. Specifically, the Asakawa patent teaches processing of settled condition codes in a pipeline. See column 5, lines 50-61. The Asakawa patent does not disclose "a plurality of first flag selectors...a second flag selector accepting a plurality of said flags... and selecting one of said flags". Accordingly, withdrawal of the rejection of claim 2 is respectfully requested.

With specific reference to claim 3, the Office Action suggests that the Runaldue patent teaches use of program registers to store condition flags. The Runaldue patent, however, does not supply the teachings absent from the combination of the Kamiyama and Vidwans patent to render claim 1 obvious. The Runaldue patent is directed to a method and apparatus for selective access to diagnostic information without increasing a number of dedicated output pins. See column 3, lines 10-18. The programmable registers disclosed in the Runaldue patent are "OR registers" that permit use of output

pins by a number of different sources to obviate the need for additional output pins. See column 3, lines 35-40 and column 4, lines 3-5. Furthermore, the programmable registers as claimed do not store flags as suggested in the Office Action (See Office Action dated March 31, 2003 page 4, last line of clause 4). As claimed in claim 3 of the present patent application, the programmable registers are a "flag selection memory" whereby an address programmed into the programmable register directs the selectors to present the appropriate flag as an output on respective first flag selectors. Accordingly, the Runaldue patent does not supply the necessary teachings to render claim 1 and claim 3 unpatentable and withdrawal of the rejection is respectfully requested.

With specific reference to claims 4 and 5, Applicant is unable to locate specific rejections in the Office Action. Accordingly, other than the response with respect to claim 1, Applicant is unable to directly address the USPTO position for rejection of these claims. Because claim 1 is believed to be patentable and because claims 4 and 5 depend from claim 1, withdrawal of the rejection of claims 4 and 5 is respectfully requested.

With specific reference to claim 7, the Office Action cites the Ochiai patent for the proposition that it is known to include a branch address as a portion of a conditional branch instruction. Claim 7 is believed to be patentable for the same

reasons claim 1, from which claim 7 depends, is believed to be patentable. The Ochiai patent does not supply the teachings absent from the Kamiyama and Vidwans patents to render claim 1 obvious. Accordingly, withdrawal of the rejection of claim 7 is respectfully requested.

With specific reference to claims 8 and 9, the Office Action suggests that the Webb patent teaches branching on various combinations of flag settings. Because, the Webb patent does not disclose programmable flag selection memory, first flag selectors, or second flag selectors, the Webb patent does not supply the teachings absent from the Kamiyama and Vidwans patents to render claims 1 or 2 obvious. The teachings in the Webb patent that assign logical operation to different ones of the 4-bits states is insufficient to render obvious claims 8 and 9 as a whole. Accordingly, withdrawal of the rejection of claims 8 and 9 is respectfully requested.

With specific reference to claims 10 and 11, the Office Action takes Official Notice that a dual-input, single output selector/multiplexor is known in the art with inputs arranged in various configurations. The Official Notice, however, does not supply sufficient additional teachings including those mentioned with respect to claims 1 and 2 to the art already cited to render claims 10 and 11 obvious as a whole. Accordingly, withdrawal of the rejection of claims 10 and 11 is respectfully requested.

Claim 12 is rejected as rendered obvious by US Pat. No. 6,380,730 to Arkin (herein "the Arkin patent") in view of the Ochiai patent. Specifically, the Office Action suggests that the Arkin patent teaches that a set of flags are determined and stored in a register and conditional branches are performed based upon the contents of the flag register and that the Ochiai patent teaches that a conditional branch instruction carries the branch address. Claim 12 recites, "determining a set of flags upon which said conditional branch is based" and "identifying a flag selection register value for each flag in said set of flags". It is not the flags that are stored in the register. The flags should not and cannot be stored because some of the flags are based upon values and conditions that are dynamic and are determined during test operations based upon results from the device under test. See page 19, lines 11-14 of the specification. In this case, storage of flags in a register takes up an instruction cycle that is not needed in embodiments of claim 12. In order to achieve a branching condition based upon dynamic flag values and as claimed in claim 12, it is a flag selection register value that is generated and stored during the compilation process and not the flags themselves. The flag selection register value then determines during a tester state which flag is to be used for purposes of the conditional branch, but the value of the flag itself determines whether to branch or not. Neither the Arkin patent nor the

Ochiai patent teaches storing a flag selection register value to properly address one or more of the available program flags. Furthermore, the concept of storing an address to access existing flags is not suggested in any of the cited art. Accordingly, the combination of the Arkin and Ochiai patents include insufficient teachings to render claim 12 obvious and withdrawal of the rejection is respectfully requested.

Claims 13 and 14 are rejected as rendered obvious by the combination of the Arkin and Ochiai patents and further in view of US Pat. No. 5,632,023 to White ("the White patent") and US Pat. No. 5,276,776 to Grady et al. ("the Grady patent"). Claims 13 and 14 depend from claim 12, which for reasons presented above is believed to be patentable. Accordingly, claims 13 and 14 are also believed to be patentable.

With respect to claim 13, the White patent teaches flag renaming and forwarding during program execution if any dependencies in the requested flag group are resolved. Claim 13 recites "re-ordering said set of flags to a set placement format" for the purpose of achieving efficiencies without having to impose program creation rules on the user. See page 25, lines 16-20 of the Specification. The renaming and forwarding teachings in the White patent are for purposes of avoiding redundant resolution of already resolved conditions, which is distinct from the step of re-ordering flags to a set placement format during a compilation process. Accordingly, the teachings

of the White patent are insufficient to render claim 13 obvious as a whole. Claim 13 is believed to be patentable and withdrawal of the rejection is respectfully requested.

With respect to claim 14, it is believed to be patentable for the same reasons claim 12 is believed to be patentable and withdrawal of the rejection is respectfully requested.

Claim 15 is rendered obvious by the combination of the Kamiyama, Vidwans and Ochiai patents. In order to render the claim obvious, the combination of the three patents must suggest the claim as a whole to one of ordinary skill in the art. The combination of the Kamiyama, Vidwans, and the Ochiai patents do not sufficiently teach the collective elements of "a branch unit comprising a programmable flag selection memory, a plurality of first flag selectors...a second flag selector accepting a plurality of said flags and selecting one of said flags to present as a branch flag". The Kamiyama patent teaches storage of a program status word for storing flag groups to be changed in accordance with the calculation results. See column 4, lines 7-10 of the Kamiyama patent. There is no such flag group storage and changing in the present claim. Claim 15 recites "a programmable flag selection memory". Accordingly, it is a value that selects the appropriate flags that is stored and not the flags themselves. The Vidwans patent in Figure 9 teaches an instruction pointer logic circuit 100. The Vidwans patent does not teach flag processing for purposes of conditional branching.

Applicant does not dispute that multiplexors are known. Applicant's position is that the use of the selectors relative to the flags and access to the flags for purposes of processing a conditional branch is not taught or suggested in the cited art. No where in the Vidwans patent is there a suggestion that would cause one of ordinary skill in the art to combine the teachings of the Kamiyama patent and the Ochiai patents to address flag processing in a context of conditional branching without execution latency to arrive at claim 15 as a whole. The Ochiai patent merely suggests that a branch address may be part of a branch instruction. These three disclosures are insufficient to arrive at the combination as claimed. Accordingly, claim 15 is believed to be patentable over the cited references and withdrawal of the rejection is respectfully requested.

Claim 16 is rejected for the same reasons as claims 15 and 14. Claim 16 depends from claim 15 and is believed to be patentable for the same reasons claim 15 is believed to be patentable. Withdrawal of the rejection is respectfully requested.

Claim 17 is rejected as rendered obvious by the Kamiyama, Vidwans and Ochiai patents and further in view of US Pat. No. 6,272,599 to Prasanna ("the Prasanna patent"). Without a specific cite in the Prasanna patent, Applicant is unable to fully identify the portion of the teachings in the Prasanna

patent that render claim 17 unpatentable. The Prasanna patent is directed to a method for improving performance in computers with cache-based architectures by adding a cache/no-cache bit to each datum thereby permitting selective cacheing of data and instructions. See column 2, lines 23-29. By contrast, the b1not0 bit in the program instruction of claim 17 does not apply to whether or not to cache, but indicates whether the logical operation has been converted from a disjunctive operation as originally programmed by a user to a more efficient conjunctive operation. It is generally known that bits represent a true or false state. The Applicant is unclear, therefore, how the Prasanna teachings offer additional suggestion and motivation to one of ordinary skill in the art of how to modify the teachings in the Kamiyama, Vidwans and Ochiai patents to arrive at claim 17. Accordingly, withdrawal of the rejection of claim 17 is respectfully requested and allowance is solicited.

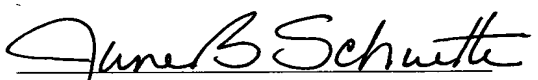
Claim 18 is rejected as rendered obvious by the Kamiyama, Vidwans, and Ochiai patents and further in view of US Pat. No. 5,534,799 to Akiyama ("the Akiyama patent"). The Akiyama patent teaches a flag control circuit to determine a final branch point even with a data signal having a bit length longer than a bit length that can be processed by an ALU. Other than showing that information coming from an ALU may be used for the purposes of branching, it is unclear what additional teachings are used for purposes of rejecting claim 18. Therefore, claim 18 is believed

to be patentable for the same reasons claim 15, from which it depends, is believed to be patentable and withdrawal of the rejection is respectfully requested.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,

Alan Krech et al.
Applicant(s)



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